

Appl. No. 10/004,010
Amdt. dated January 4, 2005
Reply to Office Action of October 5, 2004

Please replace the Abstract, beginning at page 23, line 2, with the following rewritten paragraph:

~~Efficient~~ A digital signal processor for computing various types of computation of
complex long-multiplication results and an efficient calculation of a covariance matrix are is
described. A parallel array VLIW~~The digital signal processor operates in conjunction with~~
registers, a multiplier, an adder, and a multiplexer is employed, along with specialized complex
long-multiplication instructions and communication operations between the processing elements
which are overlapped with computation to provide very high performance operation. Successive
iterations of a loop of tightly packed VLIWs may be used allowing the complex multiplication
pipeline hardware to be efficiently used. The Registers store first and second complex
operands. The multiplier simultaneously performs multiplications to produce each combination
of products between the real and imaginary terms of the first and second complex operands. The
multiplexer selects which produced products are added to or subtracted from each other based on
the type of complex multiplication being performed. The adder simultaneously performs
additions and subtractions, if necessary, to produce both real and imaginary results depending on
whether the type of complex multiplication being performed is a conjugated operation. The
registers store the results of the complex multiplication.